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EXAMINER	
MOORE JR, MICHAEL J	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,407	CHU, TAM-ANH	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,17-27 and 33-43* is/are rejected.

7)☒ Claim(s) *12-16,28-32 and 44-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Amendments made to claims **2, 18, and 34** to obviate the 35 USC 112 rejections of the previous Office Action are proper and have been entered. These rejections have been withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43** are rejected under 35 U.S.C. 102(b) as being anticipated by Hochschild et al. (U.S. 5,546,391) ("Hochschild"). Hochschild teaches all of the limitations of the listed claims with the reasoning that follows.

Regarding claim **1**, "a buffer memory of a first type to store data associated with a connection identifier corresponding to a channel in a network" is anticipated by the chunk storage RAM 715 shown in Figure 8 that stores data associated with address information (connection identifier) corresponding to an output port, which is stored in registers 730 of Figure 7. "The data being organized into at least one chunk based on a linked list" is anticipated by the linked lists of message chunks stored in chunk storage RAM 715 as spoken of on column 23, lines 29-30. "The connection identifier identifying a connection in the channel" is anticipated by the address information (connection

identifier) stored in registers 730 of Figure 7 that indicates a location in message pointer RAM 720 of the first message to be transferred to a corresponding output port (connection). "The data being part of a data stream associated with the connection" is anticipated by the messages associated with corresponding output ports spoken of on column 23, lines 29-32. Lastly, "a packet memory of a second type coupled to the buffer memory to provide access to the stored data when a transfer condition occurs" is anticipated by the continuation chunk pointer RAM 740 (packet memory) of Figure 8 coupled to chunk storage RAM (buffer memory) 715 that provides a pointer of the next successive chunk to chunk storage RAM 715 when transferring chunks to a particular output port as spoken of on column 23, line 61 – column 24, line 4.

Regarding claim **2**, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by the message pointer RAM 720 of Figure 8 that stores an address of the leading chunk associated with different messages as spoken of on column 23, lines 36-47. Lastly, "a controller coupled to the descriptor memory and the buffer memory to control data transfer between the buffer memory and the packet memory using the descriptor information" is anticipated by control circuitry 830 shown in Figure 8.

Regarding claims **8 and 40**, "an ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size" is anticipated by receiver 310 of Figure 5 that buffers incoming messages as spoken of on column 12, lines 2-8. Lastly, "a queue segmenter to chunk the data stream into the at least one

chunk" is anticipated by receiver 310 of Figure 5 that converts incoming messages into chunks as spoken of on column 12, lines 6-8.

Regarding claims **9 and 41**, "wherein the buffer memory comprises an input buffer memory to store the at least one chunk transferred from the queue segmenter" is anticipated by chunk storage RAM 715 of Figure 8.

Regarding claims **10 and 42**, "wherein the input buffer memory comprises a queue associated with the connection identifier, the queue having a threshold and being configured to store the at least one chunk" is anticipated by chunk storage RAM 715 of Figure 8 that contains 128 8-byte slots as shown in Figure 7.

Regarding claims **11 and 43**, "wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request" is anticipated by the transferring of chunks to a particular output port as spoken of on column 23, line 61 – column 24, line 4.

Regarding claim **17**, "storing data associated with a connection identifier corresponding to a channel in a network in a buffer memory of a first type" is anticipated by the chunk storage RAM 715 shown in Figure 8 that stores data associated with address information (connection identifier) corresponding to an output port, which is stored in registers 730 of Figure 7. "The data being organized into at least one chunk based on a linked list" is anticipated by the linked lists of message chunks stored in chunk storage RAM 715 as spoken of on column 23, lines 29-30. "The connection identifier identifying a connection in the channel" is anticipated by the address information (connection identifier) stored in registers 730 of Figure 7 that indicates a

location in message pointer RAM 720 of the first message to be transferred to a corresponding output port (connection). "The data being part of a data stream associated with the connection" is anticipated by the messages associated with corresponding output ports spoken of on column 23, lines 29-32. Lastly, "providing access to the stored data using a packet memory of a second type when a transfer condition occurs" is anticipated by the continuation chunk pointer RAM 740 (packet memory) of Figure 8 coupled to chunk storage RAM (buffer memory) 715 that provides a pointer of the next successive chunk to chunk storage RAM 715 when transferring chunks to a particular output port as spoken of on column 23, line 61 – column 24, line 4.

Regarding claim **18**, "storing descriptor information corresponding to the at least one chunk in a descriptor memory" is anticipated by the message pointer RAM 720 of Figure 8 that stores an address of the leading chunk associated with different messages as spoken of on column 23, lines 36-47. Lastly, "controlling data transfer between the buffer memory and the packet memory using the descriptor information" is anticipated by control circuitry 830 shown in Figure 8 that controls the operation of the individual components forming the central queue as stated on column 24, lines 40-44.

Regarding claim **24**, "buffering the data stream of a packet from an ingress of the channel by an ingress queue, the packet having a packet size" is anticipated by receiver 310 of Figure 5 that buffers incoming messages as spoken of on column 12, lines 2-8. Lastly, "segmenting the data stream into the at least one chunk" is anticipated by

receiver 310 of Figure 5 that converts incoming messages into chunks as spoken of on column 12, lines 6-8.

Regarding claim **25**, "storing the at least one chunk transferred from the queue segmenter in an input buffer memory" is anticipated by chunk storage RAM 715 of Figure 8.

Regarding claim **26**, "storing the at least one chunk in a queue associated with the connection identifier, the queue having a threshold" is anticipated by chunk storage RAM 715 of Figure 8 that contains 128 8-byte slots as shown in Figure 7.

Regarding claim **27**, "wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request" is anticipated by the transferring of chunks to a particular output port as spoken of on column 23, line 61 – column 24, line 4.

Regarding claim **33**, "a channel in a network having an ingress and egress" is anticipated by the inputs $X_1 - X_8$ and outputs $OUT_1 - OUT_8$ of the switching circuit 25 of Figure 3A. "A data buffer circuit coupled to the channel to buffer data transmitted over the channel" is anticipated by central queue 350 shown in Figure 3A. "An input buffer memory of a first type to store data associated with a connection identifier corresponding to the channel" is anticipated by the chunk storage RAM 715 shown in Figure 8 that stores data associated with address information (connection identifier) corresponding to an output port, which is stored in registers 730 of Figure 7. "The data being organized into at least one chunk based on a linked list" is anticipated by the

linked lists of message chunks stored in chunk storage RAM 715 as spoken of on column 23, lines 29-30.

"The connection identifier identifying a connection in the channel" is anticipated by the address information (connection identifier) stored in registers 730 of Figure 7 that indicates a location in message pointer RAM 720 of the first message to be transferred to a corresponding output port (connection). "The data being part of a data stream associated with the connection" is anticipated by the messages associated with corresponding output ports spoken of on column 23, lines 29-32. "An output buffer memory of the first type to store the data transferred from the input buffer memory" is anticipated by transmitter 380 shown in Figure 6. Lastly, "a packet memory of a second type coupled to the input and output buffer memories to provide access to the stored data when a transfer condition occurs" is anticipated by the continuation chunk pointer RAM 740 (packet memory) of Figure 8 coupled to chunk storage RAM (buffer memory) 715 that provides a pointer of the next successive chunk to chunk storage RAM 715 when transferring chunks to a particular output port as spoken of on column 23, line 61 – column 24, line 4.

Regarding claim **34**, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by the message pointer RAM 720 of Figure 8 that stores an address of the leading chunk associated with different messages as spoken of on column 23, lines 36-47. Lastly, "a controller coupled to the descriptor memory and the input and output buffer memories to control data transfer

between the buffer memories and the packet memory using the descriptor information" is anticipated by control circuitry 830 shown in Figure 8.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **3-7, 19-23, and 35-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochschild et al. (U.S. 5,546,391) ("Hochschild") in view of Herring et al. (U.S. 6,542,502) ("Herring").

Regarding claims **3, 19, and 35,** Hochschild teaches the apparatus of claim **2,** the method of claim **18**, and the system of claim **34**, respectively. Hochschild also teaches slots in chunk storage RAM where data chunks are stored. Hochschild fails to explicitly teach storing chunk information associated with the linked list in a chunk header. However, Herring teaches a next chunk field 304 (chunk header) associated with the data field of a chunk as shown in Figure 3. This field indicates the next chunk in the linked list. At the time of the invention, it would have been obvious to someone skilled in the art to combine the chunk header field of Herring with the teachings of Hochschild in order to provide a way to order the packets within each packet queue as spoken of on column 3, lines 6-22 of Herring.

Regarding claims **4, 20, and 36,** Hochschild further teaches continuation chunk pointer RAM 740 of Figure 8 that provides pointers to chunk storage RAM 715

indicating a successive chunk in the linked list as spoken of on column 23, line 61 – column 24, line 4.

Regarding claims **5, 21, and 37,** Hochschild further teaches a leading message chunk on column 23, lines 42-46.

Regarding claims **6, 22, and 38,** Hochschild further teaches message pointer RAM used to store an address of the leading chunk associated with different messages as spoken of on column 23, lines 35-47.

Regarding claims **7, 23, and 39,** Hochschild further teaches registers 730 of Figure 7 that each store the address of a location in message pointer RAM 720 for the first message to be transferred for the corresponding output port as spoken of on column 23, lines 53-59.

Allowable Subject Matter

5. Claims **12-16, 28-32, and 44-48** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim **12**, Hochschild (U.S. 5,546,391) teaches the apparatus of claim **11**. Hochschild fails to teach a data combiner for combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claims **13-16**, these claims are further limiting to claim **12** and are thus also allowable over the prior art of record.

Regarding claim **28**, Hochschild (U.S. 5,546,391) teaches the method of claim **27**. Hochschild fails to teach combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claims **29-32**, these claims are further limiting to claim **28** and are thus also allowable over the prior art of record.

Regarding claim **44**, Hochschild (U.S. 5,546,391) teaches the system of claim **43**. Hochschild fails to teach a data combiner for combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claim **45**, Hochschild (U.S. 5,546,391) teaches the system of claim **42**. Hochschild fails to teach an ordered list of pointers associated with the chunk headers that is transferred to the output buffer memory at a location pointed to by the head pointer as well a read circuit to burst transfer the contiguous data block from the packet memory to the output buffer memory using the ordered list of pointers.

Regarding claims **46-48**, these claims are further limiting to claim **45** and are thus also allowable over the prior art of record.

Response to Arguments

7. Applicant's arguments with respect to claims **1-11, 17-27, and 33-43** have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments with respect to claims **12-16, 28-32, and 44-48** have been fully considered and are persuasive. These rejections have been withdrawn.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sang et al. (U.S. 6,401,147) and Naven (U.S. 5,936,956) are both references that contain material pertinent to this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mjm MM

FRANK DUONG
PRIMARY EXAMINER

Michael J. Moore, Jr.
Examiner
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